

REMARKS

Applicants have canceled claim 13, without prejudice or disclaimer of its subject matter, and added new claims 14-16 to protect additional aspects of the present invention. Upon entry of this Amendment, claims 1-12 and 14-16 remain pending and under current examination.

Regarding the Office Action:

In the Office Action, the Examiner rejected claims 1 and 11 under 35 U.S.C. § 102(b) as being anticipated by “admitted prior art” (“APA”); rejected claims 1-12 under 35 U.S.C. § 102(b) as being anticipated by Rahim (U.S. Patent No. 6,362,525) (“Rahim”). Applicants traverse the rejections for the following reasons.¹

Rejection of Claims 1 and 11 under 35 U.S.C. § 102(b):

Applicants traverse the rejection of claims 1 and 11 under 35 U.S.C. § 102(b) as being anticipated by APA. Applicants respectfully disagree with the Examiner’s arguments and conclusions.

In order to properly establish that APA anticipates Applicants’ claimed invention under 35 U.S.C. § 102, each and every element of each of the claims in issue must be found, either expressly described or under principles of inherency, in that single reference. Furthermore, “[t]he identical invention must be shown in as complete detail as is contained in the ... claim.” See M.P.E.P. § 2131, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

¹ The Office Action may contain statements characterizing the related art, case law, and the claims. Regardless of whether any such statements are specifically identified herein, Applicants decline to automatically subscribe to any statements in the Office Action.

APA does not disclose each and every element of Applicants' claimed invention, despite the Examiner's allegations. In the rejection, the Examiner alleged that APA "discloses a semiconductor device, as shown in figs. 21-22 of the pending application..." (Office Action, p. 3).

It is clear, however, that APA does not disclose each and every element of Applicants' independent claims 1 and 11. Applicants' independent claim 1 recites, in part:

a second semiconductor chip provided on said wiring board at a position facing a side of said semiconductor chip, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring on said wiring board electrically connected to the pad of said semiconductor chip.

Thus, it is clear that claim 1 calls for a semiconductor device comprising a second semiconductor chip provided on said wiring board. The second semiconductor chip *faces a side* of said semiconductor chip. Further, the second semiconductor chip has passive elements integrated therein.

In sharp contrast to the claimed invention, APA does not disclose a second semiconductor chip; rather, it discloses bypass capacitors 305. *See*, for example, Fig. 21A. The bypass capacitor 305 does not constitute Applicants' claimed "second semiconductor chip."

Moreover, APA's bypass capacitor 305 does not *face a side* of the semiconductor chip 302 shown in Fig. 21A. As used in Applicants' claims, the word "side" is a noun and means "one of the line segments that bound a polygon." McGraw-Hill Dictionary of Scientific and Technical Terms, 5th Ed., Sybil P. Parker, Editor in Chief, p. 1819. Therefore, it is clear that bypass capacitor 305 in Fig. 21A does not face *a side* of the semiconductor chip 302. *See* Figs. 21A and 21B.

Finally, Applicants note that each of APA's bypass capacitors 305 is a discrete (e.g., "single") capacitor having a pair of ends, but is not a second semiconductor chip having passive elements integrated therein.

APA therefore does not anticipate Applicants' independent claim 1.

It is also clear that APA does not disclose each and every element of Applicants' independent claim 11. Applicants' independent claim 11 recites, in part:

an auxiliary semiconductor chip provided on said wiring board at a position facing a side of said semiconductor chip to be mounted, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to a wiring on said wiring board.

Thus, it is clear that claim 11 calls for a semiconductor device comprising an auxiliary semiconductor chip provided on said wiring board. The auxiliary semiconductor chip faces a side of said semiconductor chip to be mounted. Further, the auxiliary semiconductor chip has passive elements integrated therein.

In contrast to the claimed invention, APA does not disclose an auxiliary semiconductor chip; rather, it discloses bypass capacitors 305. *See*, for example, Fig. 21A. The bypass capacitor 305 is not Applicants' claimed "auxiliary semiconductor chip."

Moreover, as discussed above regarding claim 1, APA's bypass capacitor 305 does not face a side of the semiconductor chip 302 shown in Fig. 21A. As used in Applicants' claims, the word "side" is a noun and means "one of the line segments that bound a polygon." McGraw-Hill Dictionary of Scientific and Technical Terms, 5th Ed., Sybil P. Parker, Editor in Chief, p. 1819. Therefore, it is clear that bypass capacitor 305 in Fig. 21A does not face a side of the semiconductor chip 302. *See* Figs. 21A and 21B.

Finally, Applicants note that each of APA's bypass capacitors 305 is a discrete (e.g., "single") capacitor having a pair of ends, but is not an auxiliary semiconductor chip having passive elements integrated therein.

APA therefore does not anticipate Applicants' independent claim 11.

Independent claims 1 and 11 are therefore allowable, for the reasons argued above. Therefore, the improper 35 U.S.C. § 102(b) rejection of claims 1 and 11 should be withdrawn.

Rejection of Claims 1-12 under 35 U.S.C. § 102(b):

Applicants traverse the rejection of claims 1-12 under 35 U.S.C. § 102(b) as being anticipated by Rahim. Applicants respectfully disagree with the Examiner's arguments and conclusions.

Rahim does not disclose each and every element of Applicants' claimed invention, despite the Examiner's allegations. In the rejection, the Examiner alleged that Rahim "discloses a semiconductor device, as shown in figs. -10..." (Office Action, p. 4).

It is clear, however, that Rahim does not disclose each and every element of Applicants' independent claims 1, 9, and 11. Applicants' independent claim 1 recites, in part:

a second semiconductor chip provided on said wiring board at a position facing a side of said semiconductor chip, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring on said wiring board electrically connected to the pad of said semiconductor chip.

Thus, it is clear that claim 1 calls for a semiconductor device comprising a second semiconductor chip provided on said wiring board.

In contrast to the claimed invention, while Rahim discloses a device having a wiring board (grid array substrate 92/104), an IC 90 (a semiconductor chip) provided on said wiring

board (*See Rahim*, Figs. 9A and 10), and an inductor 26 (a vortex wiring pattern shown in plan view in Fig. 9b) or a low-loss substrate 98 provided on said wiring board (*See Fig. 10*), *Rahim* does not disclose that the inductor 26 or the low-loss substrate 98 is a semiconductor chip. For example, inductor 26 consists of a wiring pattern provided on grid array substrate 92 (*See Figs. 9A and 9B*). Moreover, low-loss substrate 98 is “a material having a low conductivity compared to that of the substrate of IC 90, and may be a ceramic material such as alumina.” *Rahim*, col. 11, lines 52-54. It is therefore clear that each of *Rahim*’s inductor 26 and low-loss substrate 98 is not a semiconductor material.

Rahim therefore does not anticipate Applicants’ independent claim 1.

It is also clear that *Rahim* does not disclose each and every element of Applicants’ independent claim 9. Applicants’ independent claim 9 recites, in part:

a plurality of semiconductor device portion units arranged in a lamination direction and each including: a wiring board; a semiconductor chip provided on said wiring board and having a pad electrically connected to a wiring on said wiring board; and a second semiconductor chip provided on said wiring board at a position facing a side of said semiconductor chip, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to the wiring on said wiring board electrically connected to the pad of said semiconductor chip; and

a vertical wiring portion passing through said wiring boards of said plural semiconductor device portion units and electrically connecting said wiring boards to one another.

Thus, it is clear that claim 9 calls for a semiconductor device comprising a plurality of semiconductor device portion units arranged in a lamination direction; and a vertical wiring portion passing through wiring boards of said plural semiconductor device portion units and electrically connecting said wiring boards to one another.

In contrast to the claimed invention, while Rahim discloses a device having a wiring board (grid array substrate 92/104), and an IC 90 (a semiconductor chip) provided on said wiring board (See Rahim, Figs. 9A and 10), Rahim does not disclose at least Applicants' claimed "a plurality of devices arranged in a lamination direction," and for at least this reason, Rahim therefore does not anticipate Applicants' independent claim 9.

It is also clear that Rahim does not disclose each and every element of Applicants' independent claim 11. Applicants' independent claim 11 recites, in part:

an auxiliary semiconductor chip provided on said wiring board at a position facing a side of said semiconductor chip to be mounted, having passive elements integrated therein, and having pads for external connection to which both ends of the passive elements are connected respectively and at least one of which is electrically connected to a wiring on said wiring board.

In contrast to the claimed invention, while Rahim discloses a device having a wiring board (grid array substrate 92/104), an IC 90 (a semiconductor chip) provided on said wiring board (See Rahim, Figs. 9A and 10), and an inductor 26 (a vortex wiring pattern shown in plan view in Fig. 9b) or a low-loss substrate 98 provided on said wiring board (See Fig. 10), Rahim does not disclose that the inductor 26 or the low-loss substrate 98 is a semiconductor chip. For example, inductor 26 consists of a wiring pattern provided on grid array substrate 92 (See Figs. 9A and 9B). Moreover, low-loss substrate 98 is "a material having a low conductivity compared to that of the substrate of IC 90, and may be a ceramic material such as alumina." Rahim, col. 11, lines 52-54. It is therefore clear that each of Rahim's inductor 26 and low-loss substrate 98 is not a semiconductor material.

APA therefore does not anticipate Applicants' independent claim 11.

Independent claims 1, 9, and 11 are therefore allowable, for the reasons argued above. Dependent claims 2-8, 10, and 12 are also allowable at least by virtue of their respective

dependence from base claim 1, 9, or 11. Therefore, the improper 35 U.S.C. § 102(b) rejection of claims 1-12 should be withdrawn.

New Claims:

Applicants have added new claims 14-16 to protect additional aspects of the present invention. Neither APA nor Rahim disclose or suggest at least the claimed "each of the pads of said second semiconductor chip electrically connected to the pad of said semiconductor chip via the wiring on said wiring board is positioned to be adjacent to said pad of said semiconductor chip." Applicants submit that claims 14-16 are also allowable over APA and Rahim.

Conclusion:

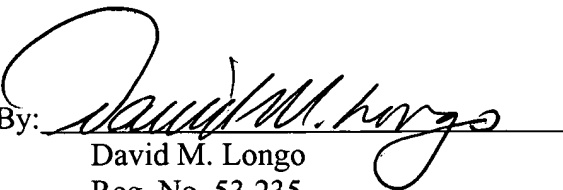
In view of the foregoing, Applicants request reconsideration of the application and withdrawal of the rejections. Pending claims 1-12 and 14-16 are in condition for allowance, and Applicants request a favorable action.

If there are any remaining issues or misunderstandings, Applicants request the Examiner telephone the undersigned representative to discuss them.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

By: 
David M. Longo
Reg. No. 53,235

Dated: September 15, 2005

/direct telephone: (202) 408-4489/